INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
51889/3	10/719,119
Douglas R. Hackler, Sr. et al.	
FILING: November 21, 2003	GROUP: 2814

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DC	A12	6,104,068	08/15/00	Forbes	257	365	09/01/98
DC	A13	6,097,221	08/01/00	Sako	326	113	12/10/96
DC	A14	6072,354	06/06/00	Tachibana et al.	327	390	09/29/97
DC	A15	4,468,574	08/28/84	Engeler et al.	307	451	05/03/82
DC	A16	4,300,064	11/10/81	Eden	307	446	02/12/79

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED
PHAT X. CAO	5/24/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PC	17	5,349,228	09/20/94	Neudeck et al.	257	365	12/07/93
PC	18	5,273,921	12/28/93	Neudeck et al.	437	41	12/27/91
PC	19	3,755,012	08/28/73	George et al.	148	175	03/19/71

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	20							
	21							
	22							
	23							
	24							
	25							
	26							
	27							

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication, etc.)

PC	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
PC	29	Wann et al., "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.
PC	30	Yang et al., "Back-Gated CMOS on SOIAS for Dynamic Threshold Voltage Control," IEEE Transactions on Electron Devices, Vol. 44, No. 5, May 1997, pgs. 822-831.
PC	31	Assaderaghi et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pgs. 414-422.

EXAMINER	PHAT X. CAO	DATE CONSIDERED	5/24/05

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